FIG.1

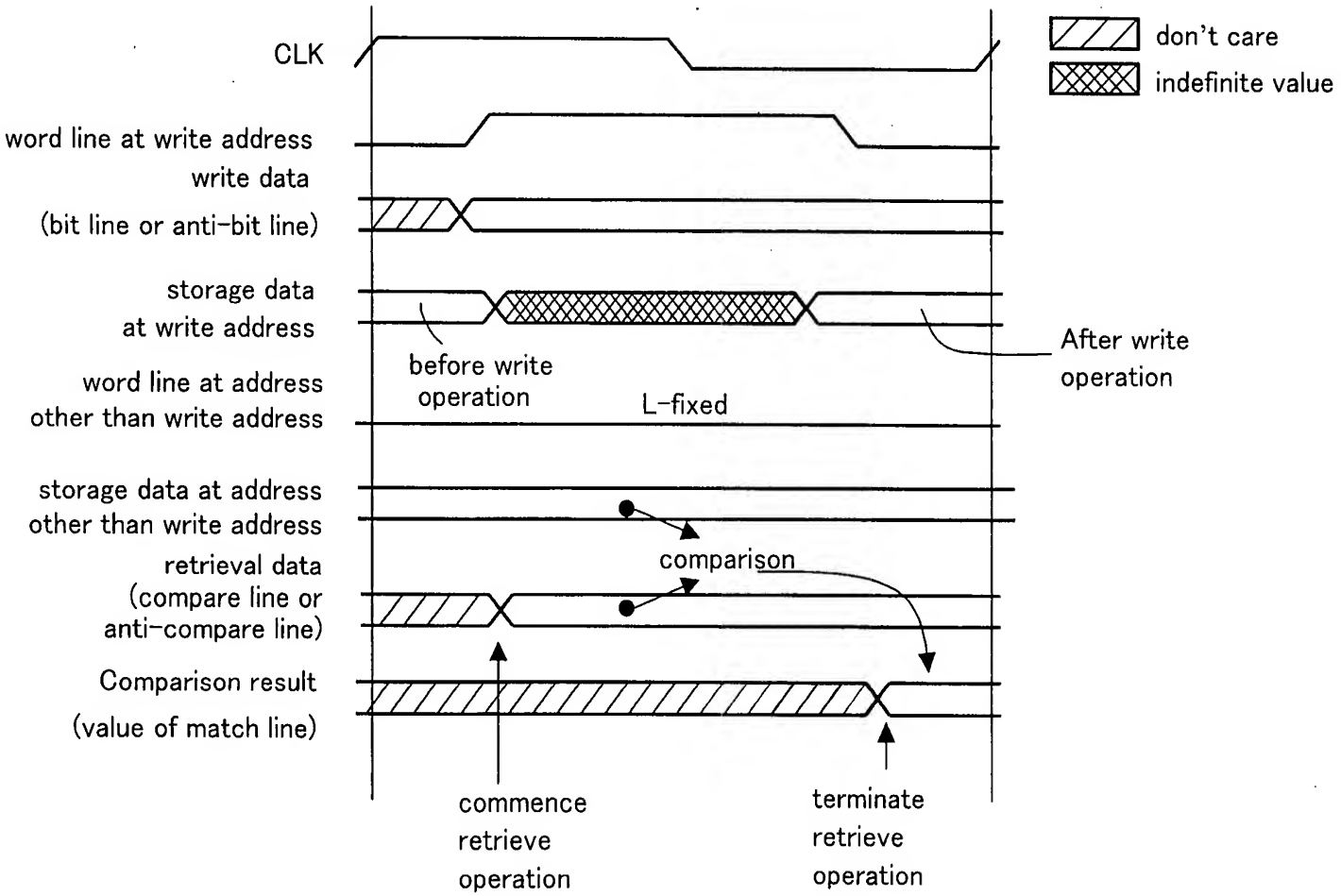

CLK
word line at write address
write data
(bit line or anti-bit line)
storage data
at write address
word line at address
other than write address
storage data at address
other than write address
retrieval data
(compare line or
anti-compare line)
Comparison result
(value of match line)
don't care
indefinite value
before write
operation
After write
operation
L-fixed
comparison
commence
retrieve
operation
terminate
retrieve
operation

FIG.2

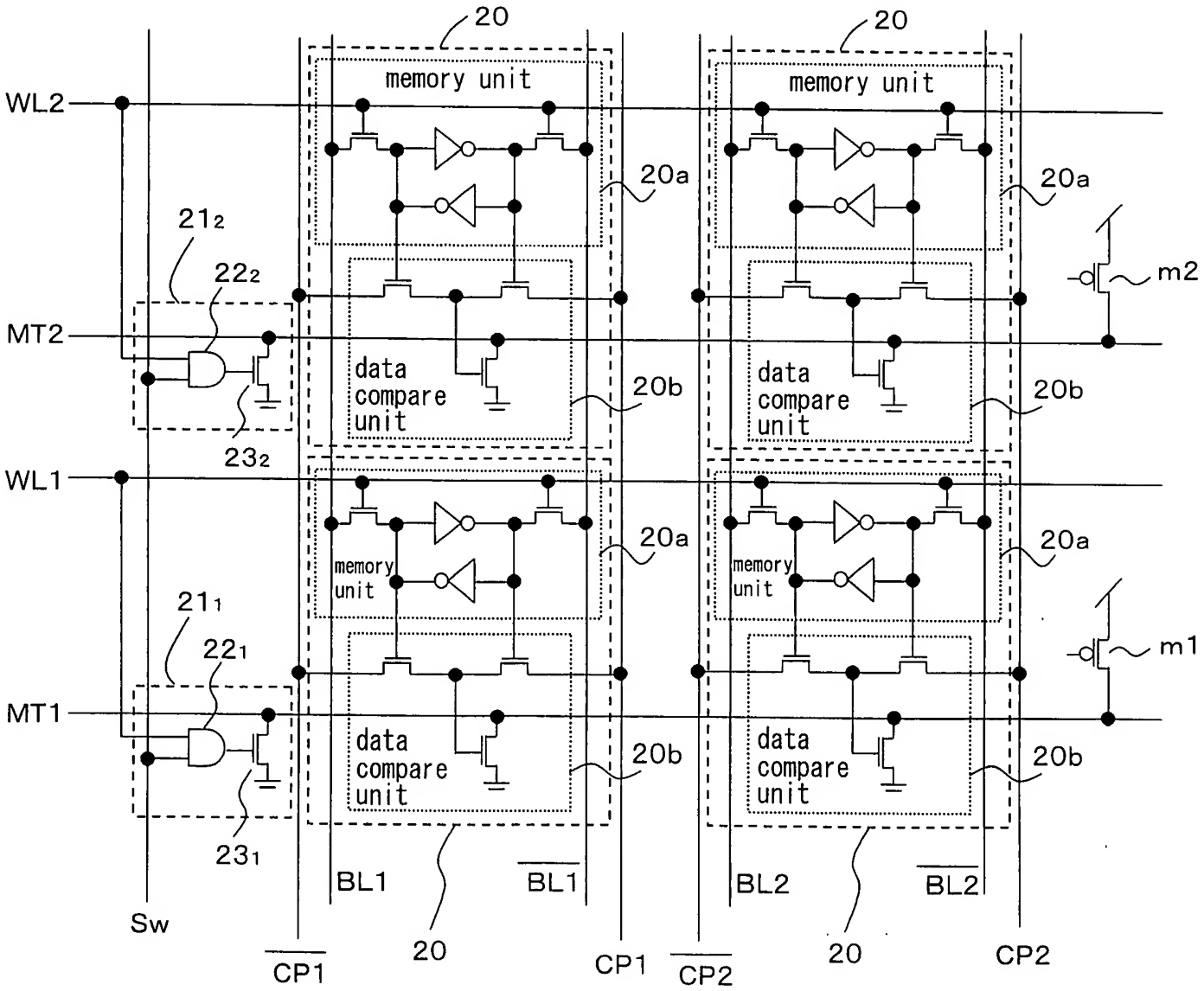

20
memory unit
WL2
20a
21₂
22₂
MT2
data
compare
unit
20b
23₂
WL1
21₁
22₁
MT1
23₁
Sw
BL1
BL1
CP1
20
CP1
BL2
BL2
CP2
20
CP2
m2
m1

FIG.3

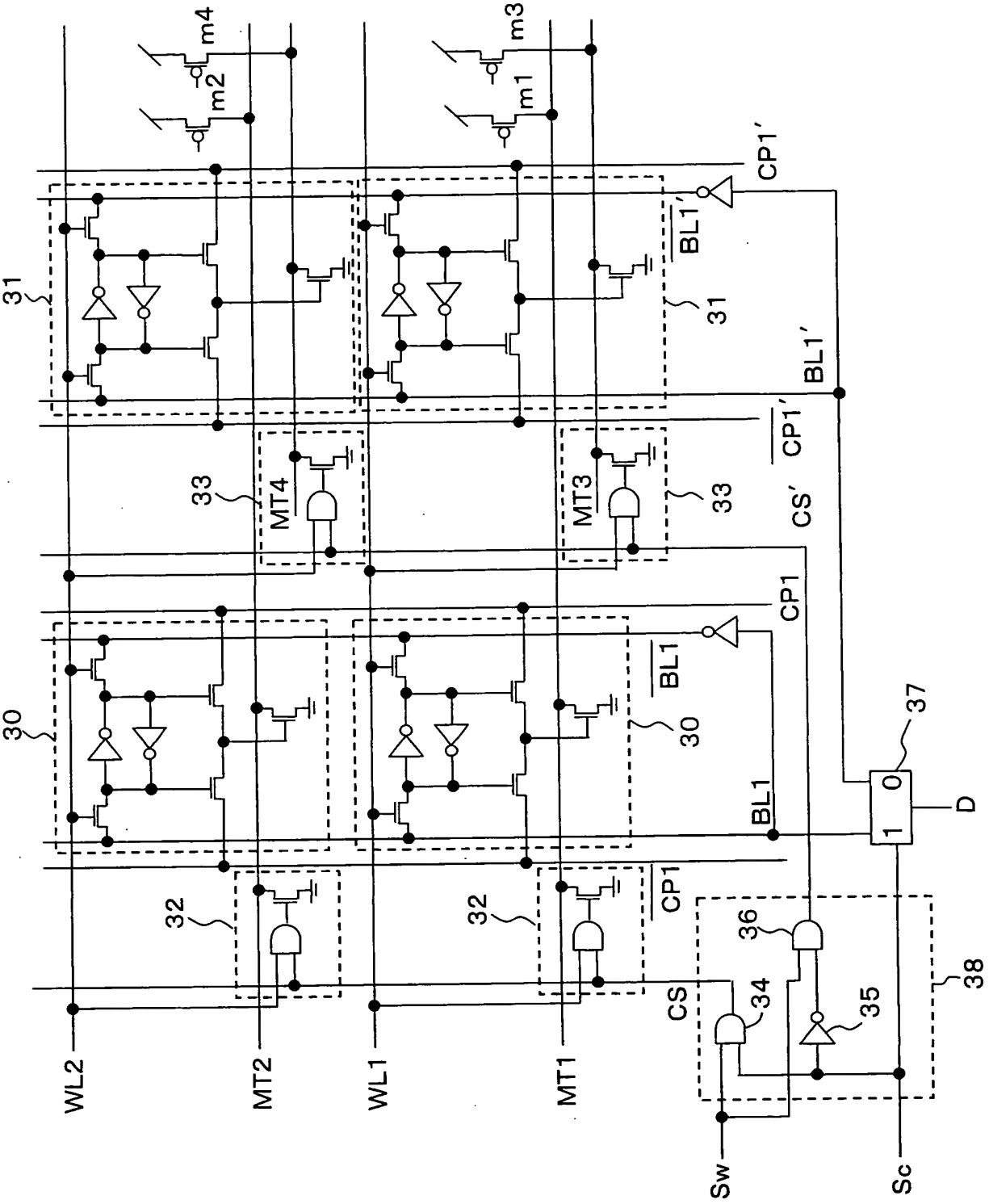

m4
m2
m3
m1
CP1'
31
BL1'
BL1'
CS'
CP1'
33
MT4
MT3
CP1
30
BL1
BL1
37
D
32
CP1
36
CS
34
35
38
WL2
MT2
WL1
MT1
Sw
Sc

FIG.4

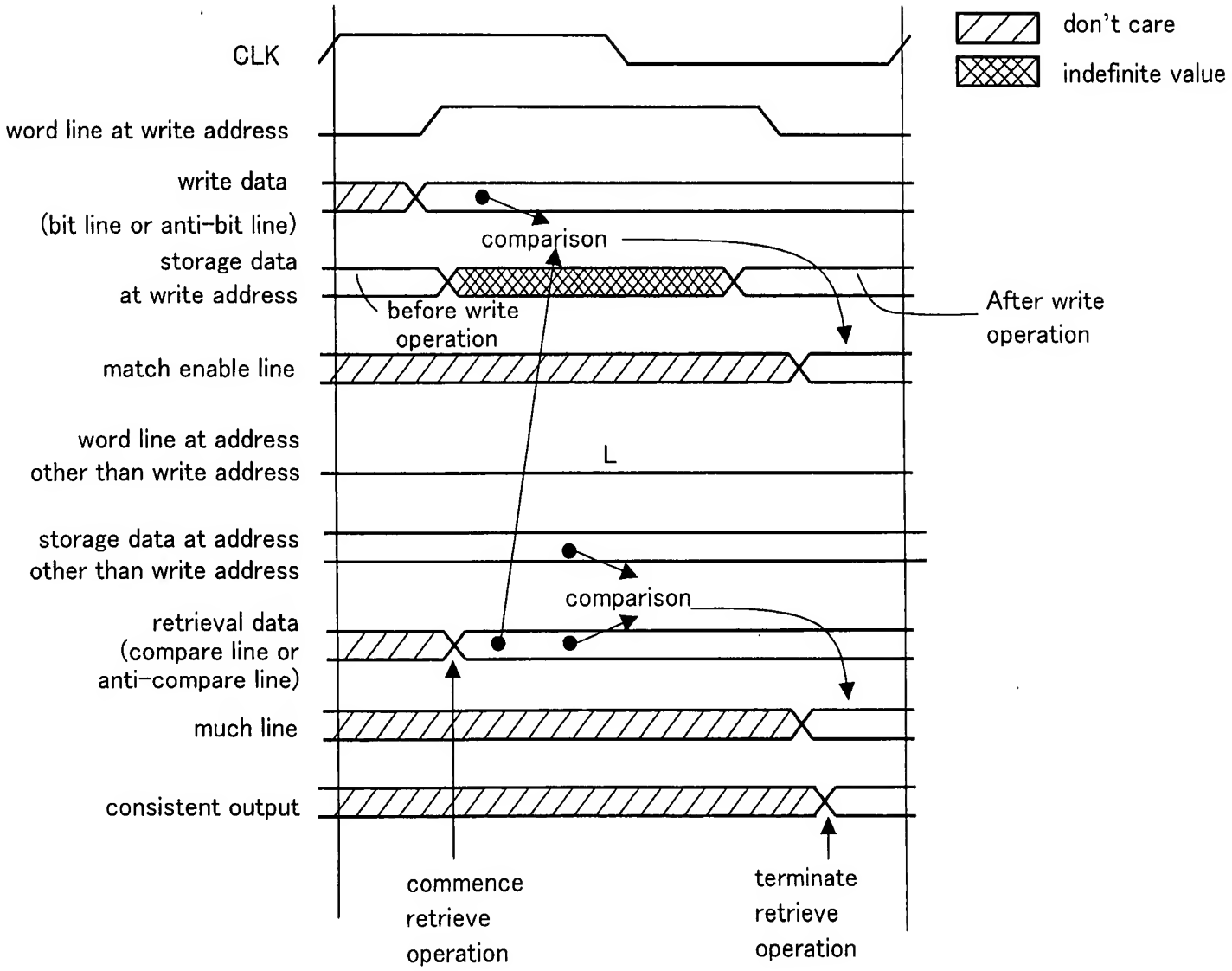

don't care
indefinite value
CLK
word line at write address
write data
(bit line or anti-bit line)
storage data
at write address
comparison
before write
operation
After write
operation
match enable line
word line at address
other than write address
L
storage data at address
other than write address
comparison
retrieval data
(compare line or
anti-compare line)
much line
consistent output
commence
retrieve
operation
terminate
retrieve
operation

FIG.5

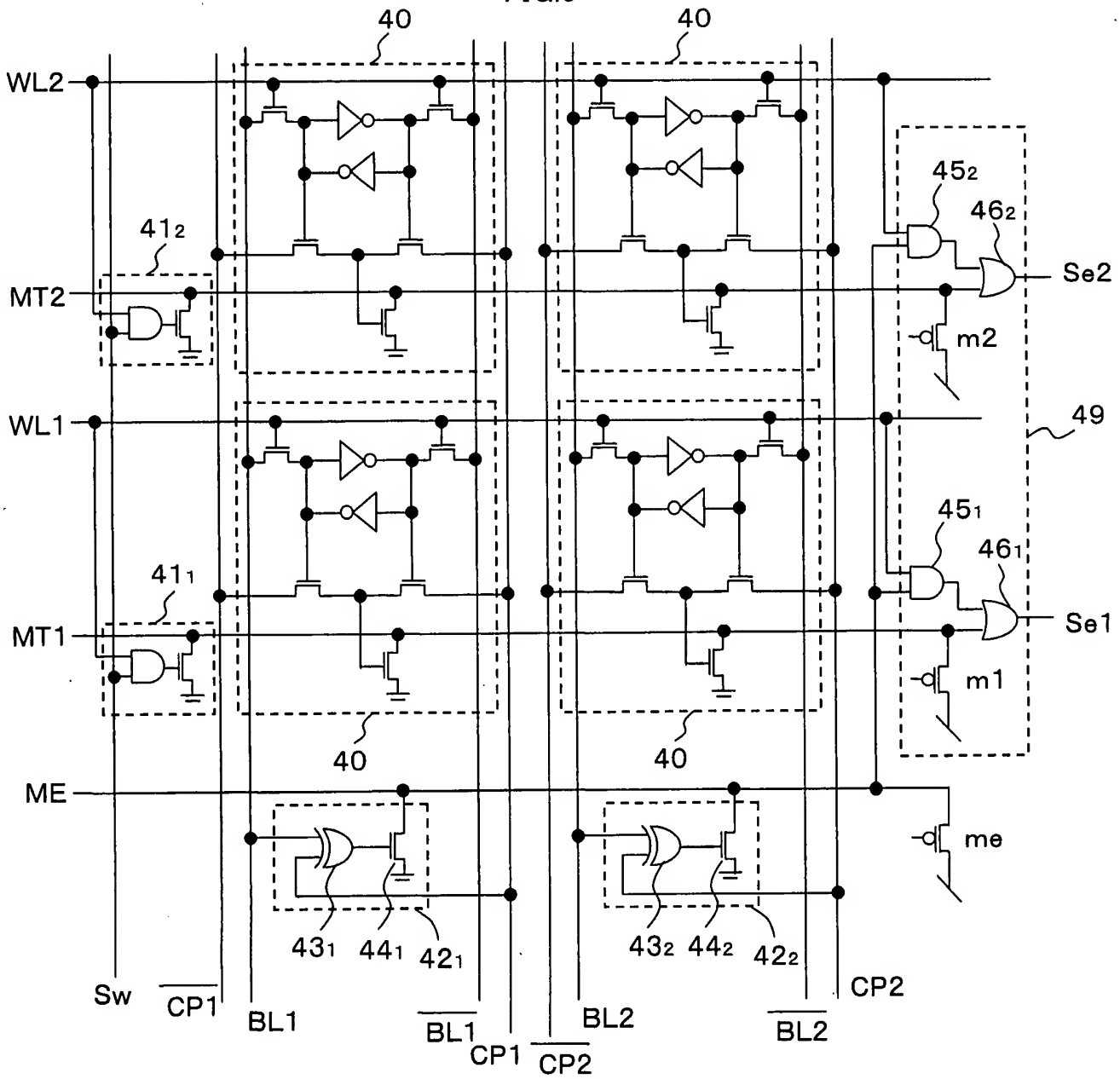

40
40
WL2
41_2
45_2
46_2
MT2
Se2
m2
WL1
49
45_1
46_1
41_1
MT1
Se1
m1
40
40
ME
me
43_1 44_1 42_1
43_2 44_2 42_2
Sw
$\overline{CP1}$
BL1
$\overline{BL1}$
CP1
$\overline{CP2}$
BL2
$\overline{BL2}$
CP2

FIG.6

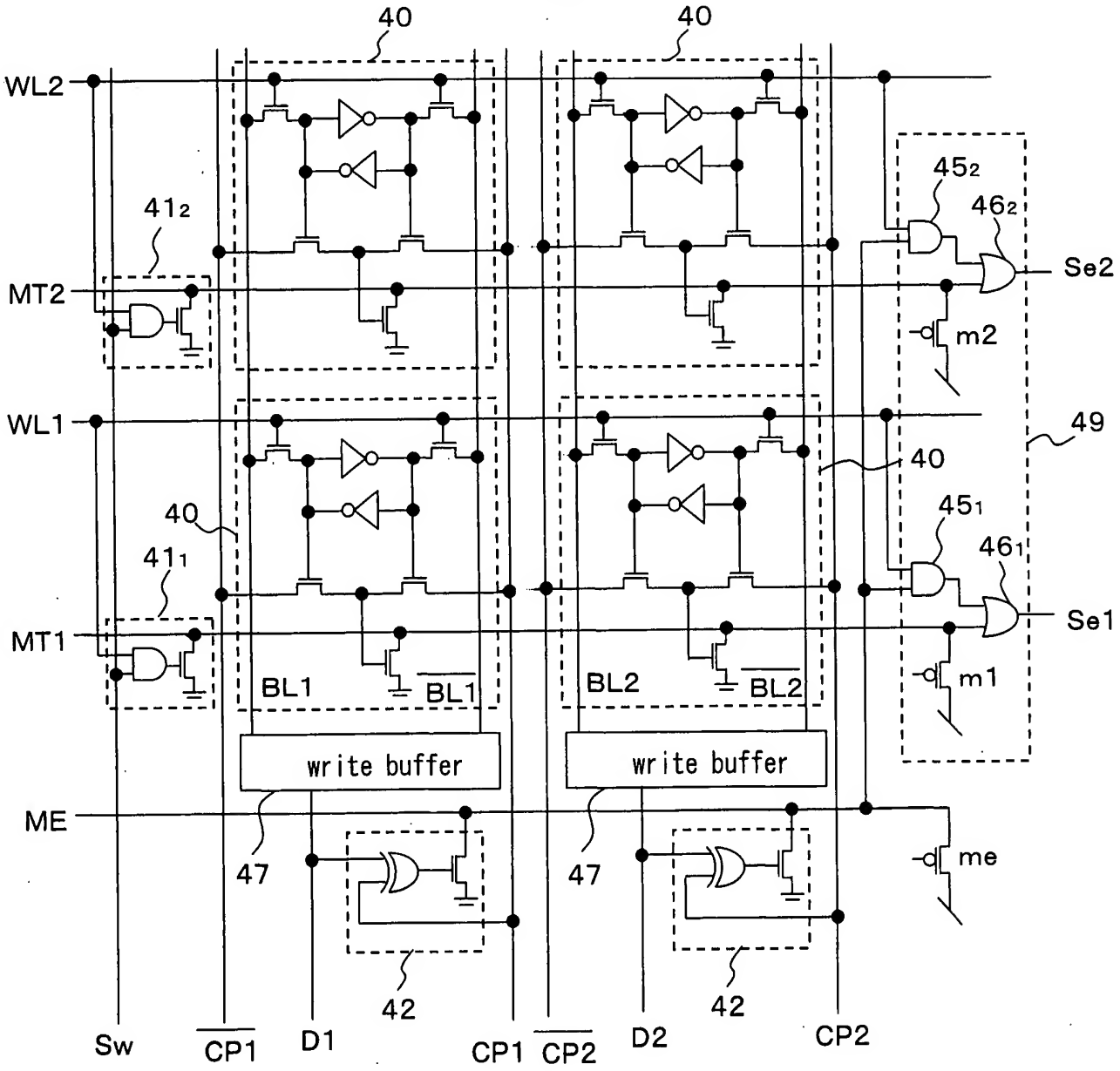

40
40
WL2
41_2
45_2
46_2
Se2
MT2
m2
WL1
49
40
40
45_1
41_1
46_1
Se1
MT1
m1
BL1
$\overline{BL1}$
BL2
$\overline{BL2}$
write buffer
write buffer
ME
me
47
47
42
42
Sw
$\overline{CP1}$
D1
CP1
$\overline{CP2}$
D2
CP2

FIG.7

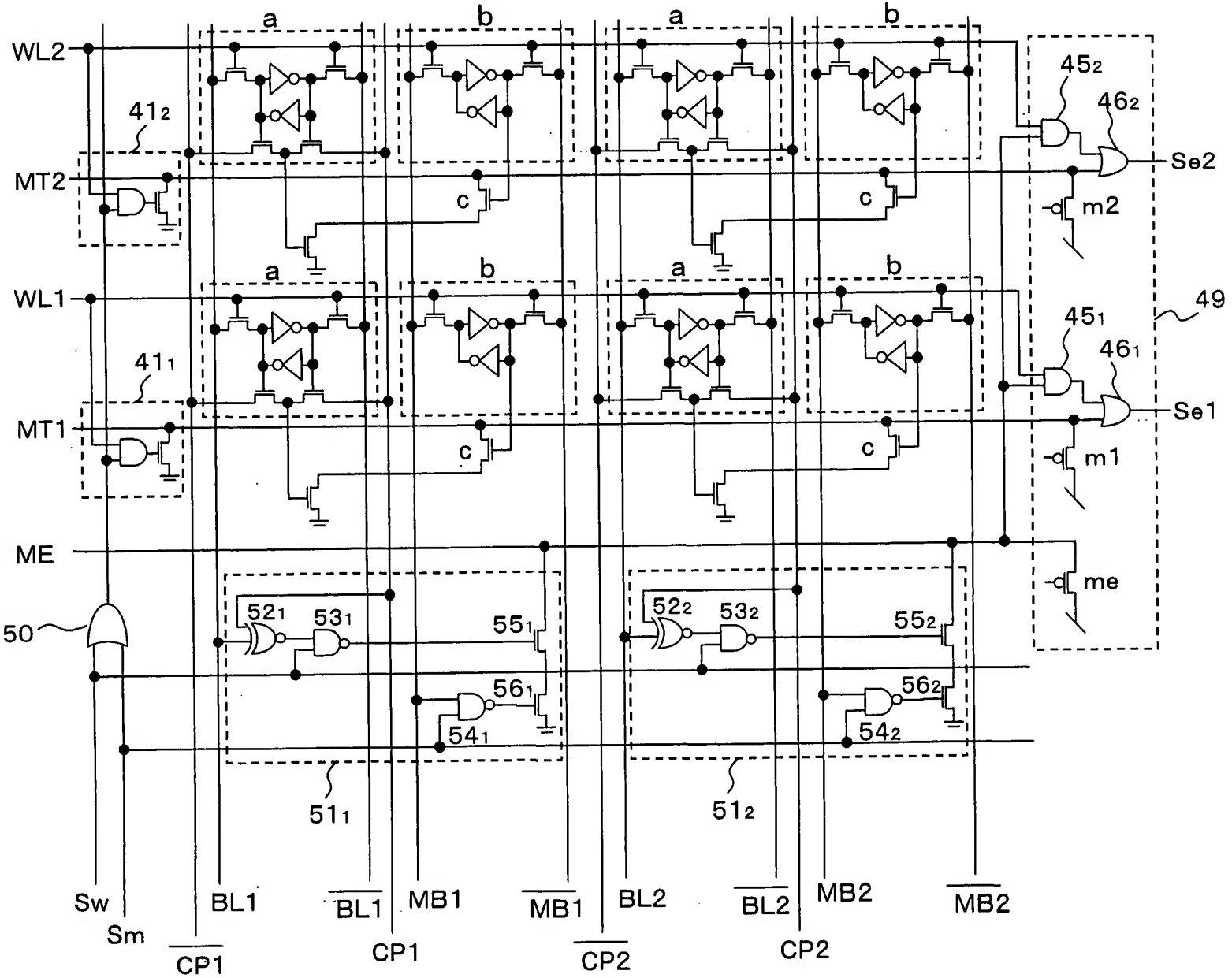

WL2
WL1
MT2
MT1
ME
50
Sw
Sm
BL1
$\overline{BL1}$
MB1
$\overline{MB1}$
BL2
$\overline{BL2}$
MB2
$\overline{MB2}$
$\overline{CP1}$
CP1
CP2
$\overline{CP2}$
a
b
c
41_2
41_1
45_2
46_2
45_1
46_1
Se2
Se1
m2
m1
me
49
52_1
53_1
55_1
56_1
54_1
51_1
52_2
53_2
55_2
56_2
54_2
51_2

FIG.8

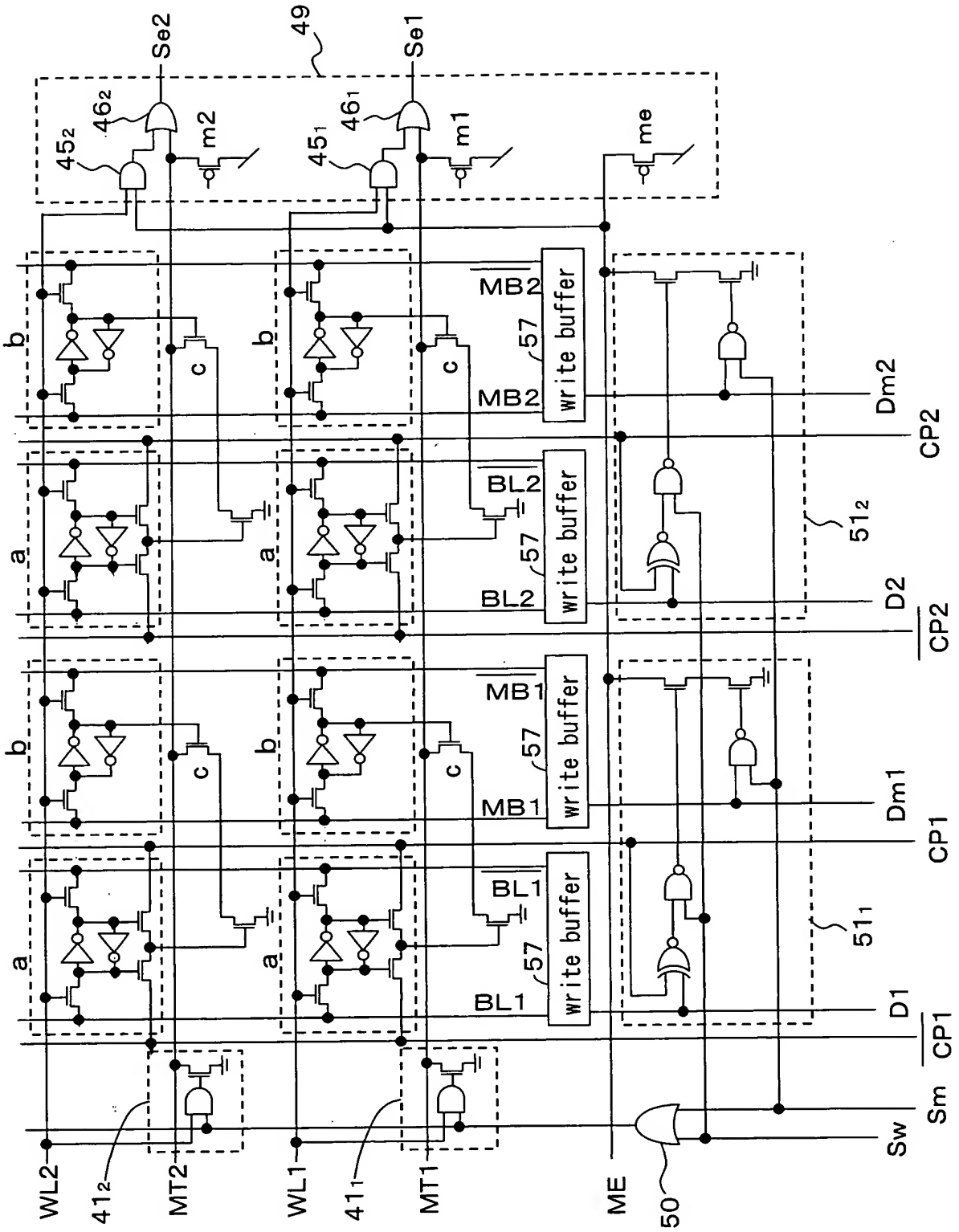

49
Se2
Se1
45_2
46_2
45_1
46_1
m2
m1
me
a
b
c
MB2
MB1
BL2
BL1
57
write buffer
Dm2
Dm1
D2
D1
CP2
CP1
51_2
51_1
WL2
WL1
41_2
41_1
MT2
MT1
ME
50
Sw
Sm

FIG.9

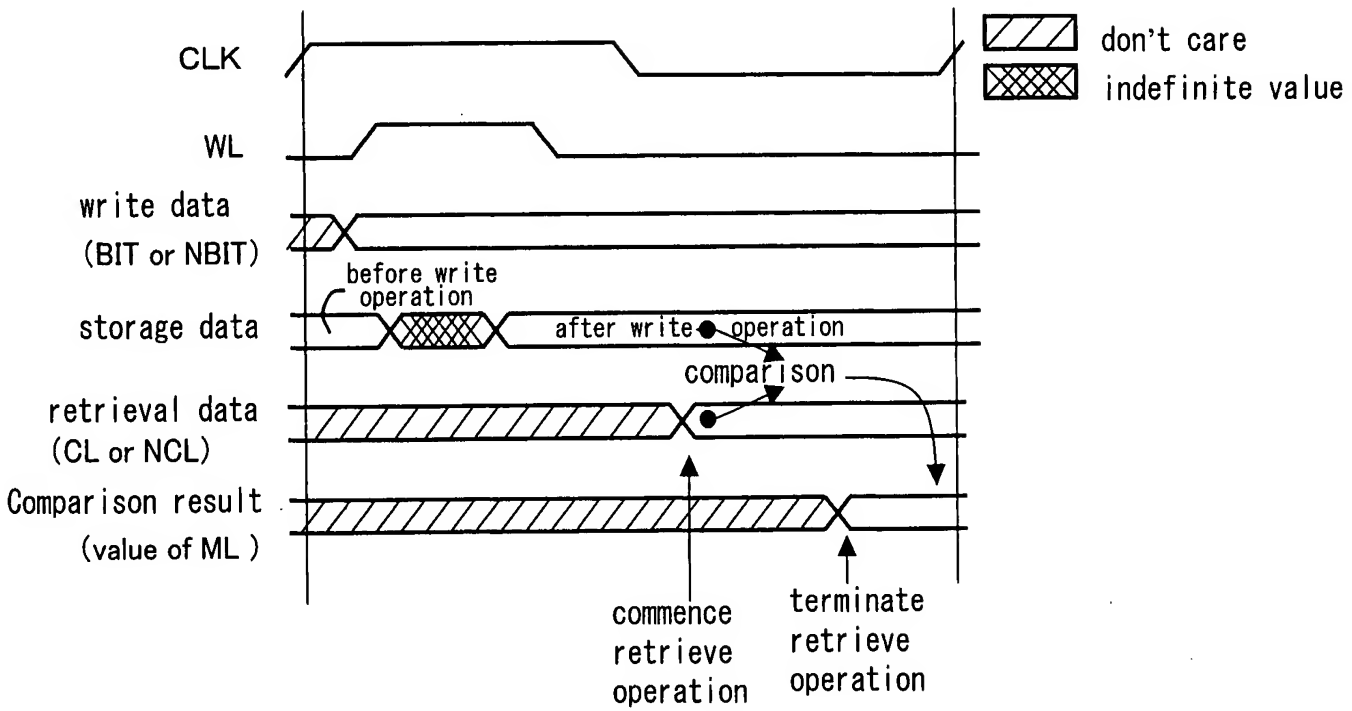

CLK
WL
write data
(BIT or NBIT)
before write operation
storage data
after write operation
comparison
retrieval data
(CL or NCL)
Comparison result
(value of ML)
commence retrieve operation
terminate retrieve operation
don't care
indefinite value

FIG.10

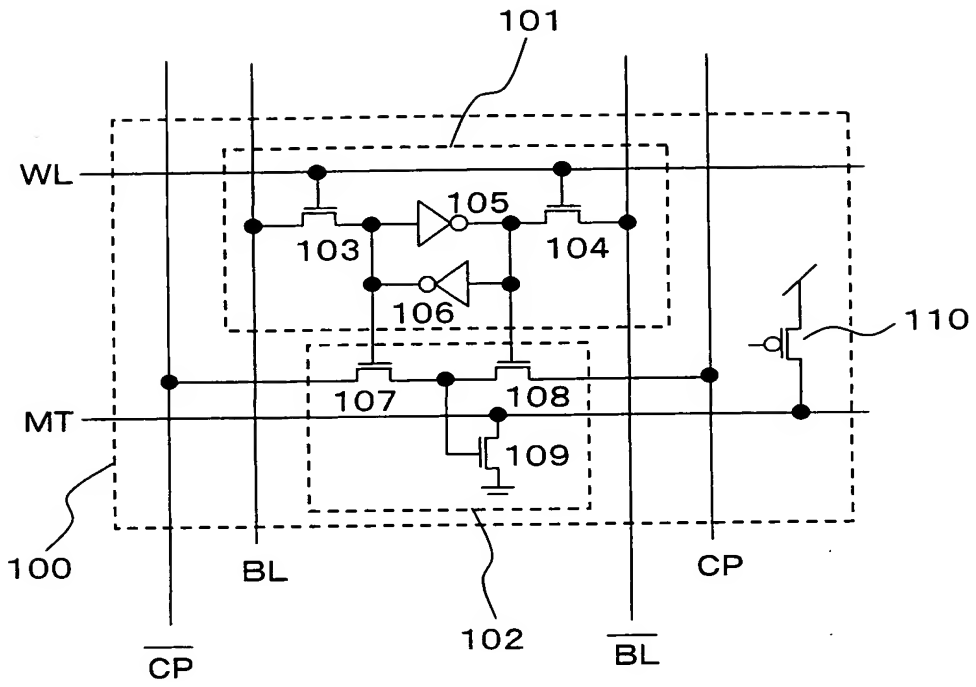

101
WL
105
103
104
106
110
107
108
MT
109
100
BL
102
CP
$\overline{CP}$
$\overline{BL}$

FIG.11

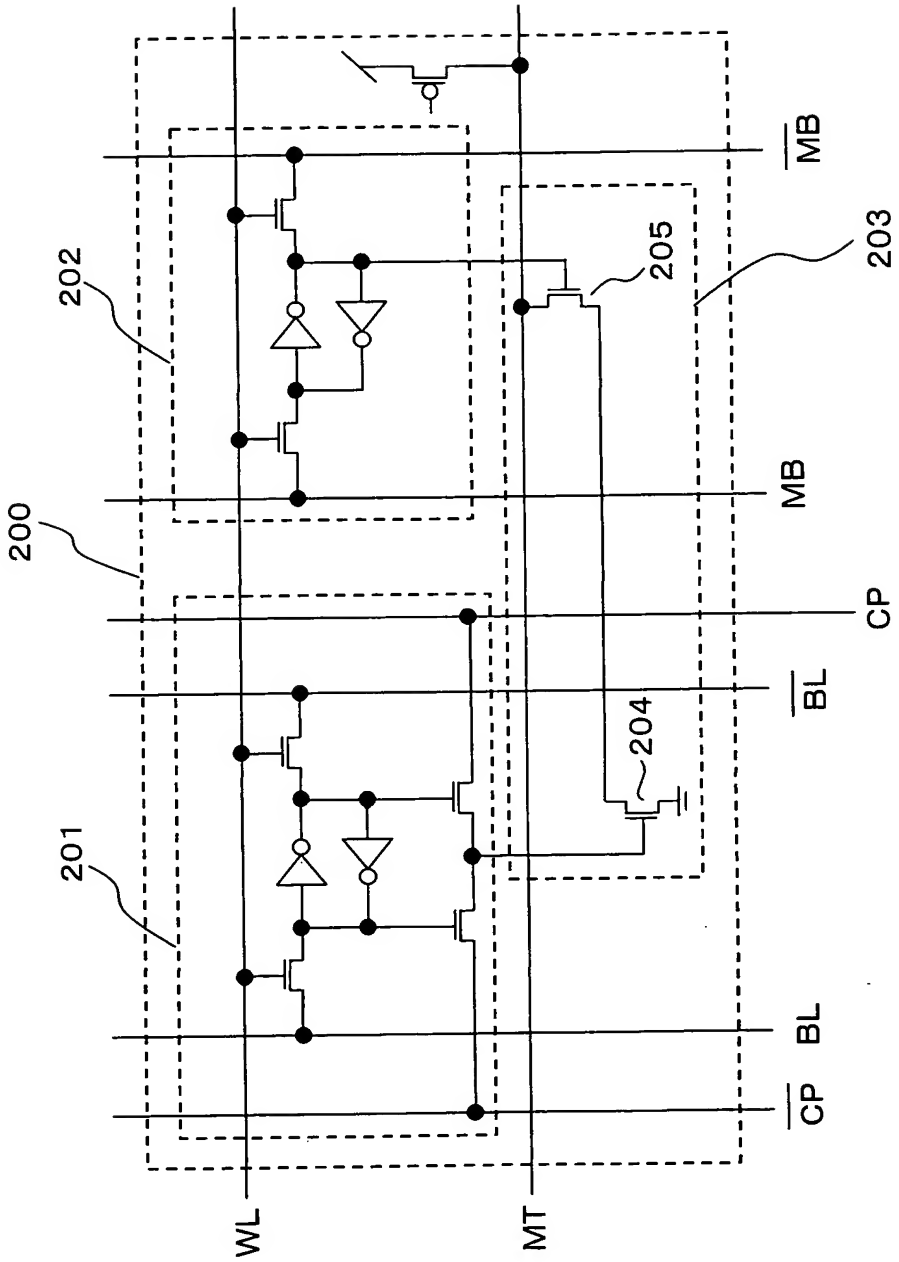

200
201
202
203
204
205
WL
MT
$\overline{CP}$
BL
$\overline{BL}$
CP
MB
$\overline{MB}$

FIG.12

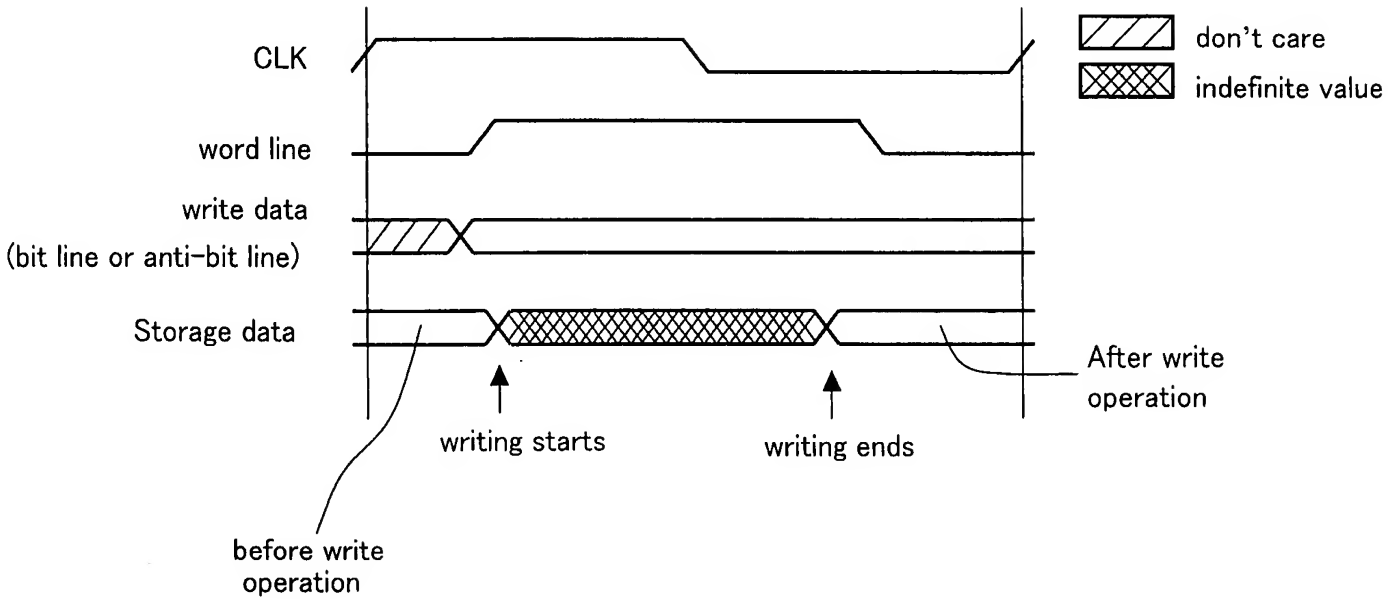

CLK
word line
write data
(bit line or anti-bit line)
Storage data
don't care
indefinite value
After write operation
writing starts
writing ends
before write operation

FIG.13

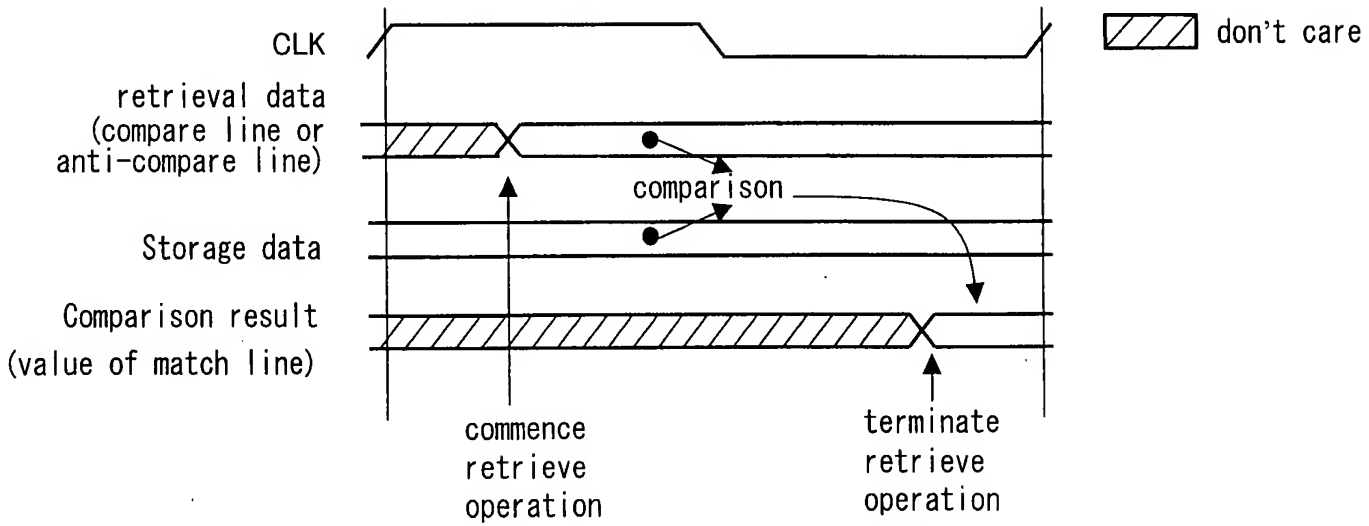
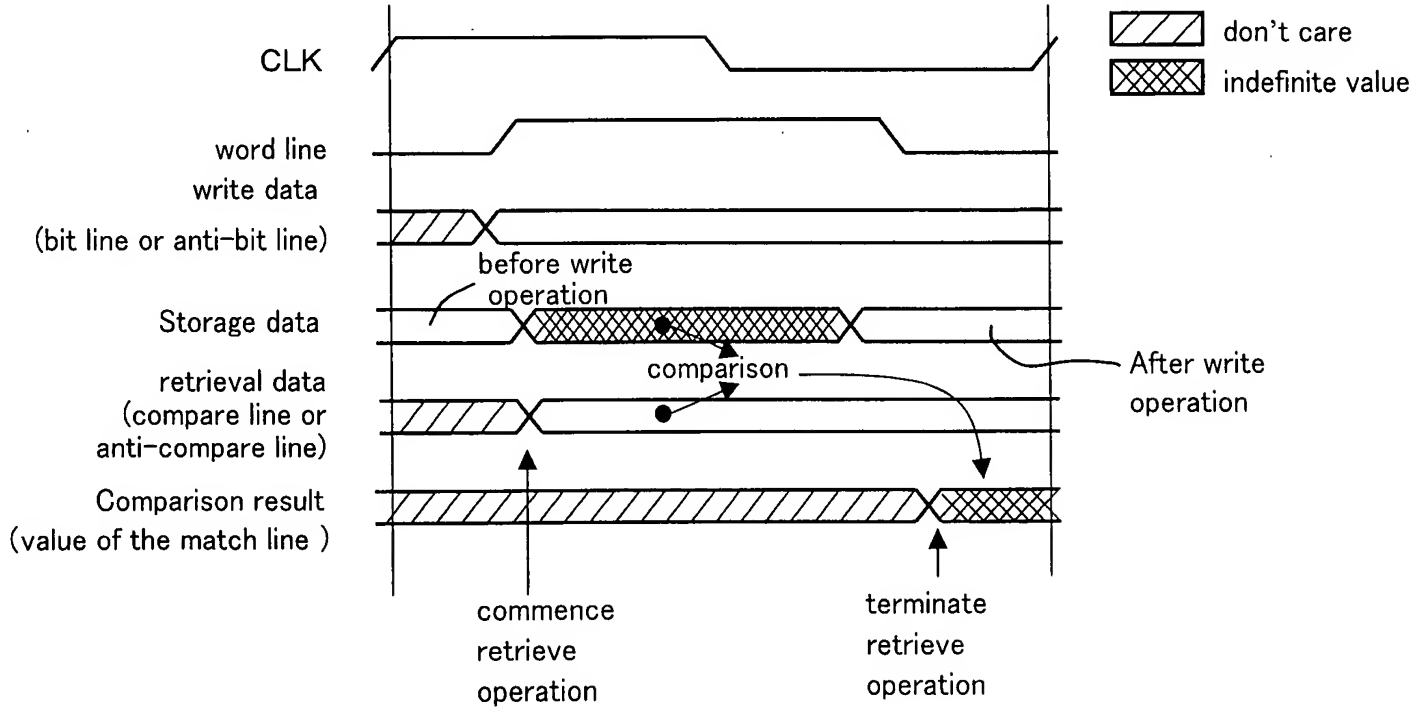

CLK
retrieval data
(compare line or
anti-compare line)
Storage data
Comparison result
(value of match line)
comparison
commence
retrieve
operation
terminate
retrieve
operation
don't care

FIG.14


CLK
word line
write data
(bit line or anti-bit line)
Storage data
retrieval data
(compare line or
anti-compare line)
Comparison result
(value of the match line)
before write
operation
comparison
After write
operation
commence
retrieve
operation
terminate
retrieve
operation
don't care
indefinite value